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\* Design Summary \*

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Top Level Output File Name : MIPS\_top\_module.ngc

Primitive and Black Box Usage:

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# BELS : 826

# GND : 1

# INV : 2

# LUT1 : 55

# LUT2 : 23

# LUT3 : 73

# LUT4 : 140

# LUT5 : 40

# LUT6 : 194

# MUXCY : 169

# VCC : 1

# XORCY : 128

# FlipFlops/Latches : 112

# FD : 71

# FDRE : 30

# FDSE : 2

# LD : 7

# LDCE : 1

# LDPE : 1

# RAMS : 15

# RAM32M : 10

# RAM32X1D : 4

# RAMB8BWER : 1

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 161

# OBUF : 161

Device utilization summary:

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Selected Device : 6slx9tqg144-3

Slice Logic Utilization:

Number of Slice Registers: 112 out of 11440 0%

Number of Slice LUTs: 575 out of 5720 10%

Number used as Logic: 527 out of 5720 9%

Number used as Memory: 48 out of 1440 3%

Number used as RAM: 48

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 578

Number with an unused Flip Flop: 466 out of 578 80%

Number with an unused LUT: 3 out of 578 0%

Number of fully used LUT-FF pairs: 109 out of 578 18%

Number of unique control sets: 9

IO Utilization:

Number of IOs: 162

Number of bonded IOBs: 162 out of 102 158% (\*)

Specific Feature Utilization:

Number of Block RAM/FIFO: 1 out of 32 3%

Number using Block RAM only: 1

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

WARNING:Xst:1336 - (\*) More than 100% of Device resources are used

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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

--------------------------------------------------------------------------------------+--------------------------+-------+

clk | BUFGP | 118 |

alu\_control/ALU\_op[1]\_PWR\_8\_o\_equal\_3\_o(alu\_control/ALU\_op[1]\_PWR\_8\_o\_equal\_3\_o<1>1:O)| NONE(\*)(alu\_control/op\_1)| 2 |

alu\_control/op\_2\_G(alu\_control/op\_2\_G:O) | NONE(\*)(alu\_control/op\_2)| 1 |

control/ALUop\_1\_G(control/ALUop\_1\_G:O) | NONE(\*)(control/ALUop\_1) | 1 |

control/Branch\_G(control/Branch\_G:O) | NONE(\*)(control/Branch) | 2 |

N0 | NONE(control/ALUsrc) | 1 |

control/MemtoReg\_G(control/MemtoReg\_G1:O) | NONE(\*)(control/MemtoReg)| 1 |

control/RegDst\_G(control/RegDst\_G:O) | NONE(\*)(control/RegDst) | 1 |

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(\*) These 6 clock signal(s) are generated by combinatorial logic,

and XST is not able to identify which are the primary clock signals.

Please use the CLOCK\_SIGNAL constraint to specify the clock signal(s) generated by combinatorial logic.

INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer\_type constraint in order to insert these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: 10.531ns (Maximum Frequency: 94.954MHz)

Minimum input arrival time before clock: No path found

Maximum output required time after clock: 8.659ns

Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clk'

Clock period: 10.531ns (frequency: 94.954MHz)

Total number of paths / destination ports: 209620 / 281

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Delay: 10.531ns (Levels of Logic = 7)

Source: pc/out\_4 (FF)

Destination: data\_mem/Mram\_mem (RAM)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: pc/out\_4 to data\_mem/Mram\_mem

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FD:C->Q 64 0.447 1.984 pc/out\_4 (pc/out\_4)

LUT5:I0->O 61 0.203 1.620 ins<21>1 (ins\_21\_OBUF)

RAM32X1D:DPRA0->DPO 3 0.205 0.651 registers/Mram\_mem61 (data1<30>\_mand)

LUT3:I2->O 7 0.205 1.002 data1<30>1 (data1\_30\_OBUF)

LUT4:I1->O 1 0.205 0.000 alu/Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_lut<15> (alu/Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_lut<15>)

MUXCY:S->O 66 0.172 1.654 alu/Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<15> (alu/Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<15>)

LUT6:I5->O 1 0.205 0.808 alu/operation[3]\_in1[31]\_select\_19\_OUT<1>1 (alu/operation[3]\_in1[31]\_select\_19\_OUT<1>1)

LUT6:I3->O 2 0.205 0.616 alu/operation[3]\_in1[31]\_select\_19\_OUT<1>3 (alu/operation[3]\_in1[31]\_select\_19\_OUT<1>)

RAMB8BWER:ADDRBRDADDR6 0.350 data\_mem/Mram\_mem

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Total 10.531ns (2.197ns logic, 8.334ns route)

(20.9% logic, 79.1% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 12735 / 145

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Offset: 8.659ns (Levels of Logic = 4)

Source: pc/out\_4 (FF)

Destination: data1<31> (PAD)

Source Clock: clk rising

Data Path: pc/out\_4 to data1<31>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FD:C->Q 64 0.447 1.984 pc/out\_4 (pc/out\_4)

LUT5:I0->O 61 0.203 1.620 ins<21>1 (ins\_21\_OBUF)

RAM32X1D:DPRA0->DPO 3 0.205 0.651 registers/Mram\_mem61 (data1<30>\_mand)

LUT3:I2->O 7 0.205 0.773 data1<30>1 (data1\_30\_OBUF)

OBUF:I->O 2.571 data1\_30\_OBUF (data1<30>)

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Total 8.659ns (3.631ns logic, 5.028ns route)

(41.9% logic, 58.1% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'control/Branch\_G'

Total number of paths / destination ports: 32 / 32

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Offset: 5.453ns (Levels of Logic = 2)

Source: control/Branch (LATCH)

Destination: pc\_in<31> (PAD)

Source Clock: control/Branch\_G falling

Data Path: control/Branch to pc\_in<31>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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LD:G->Q 35 0.498 1.563 control/Branch (control/Branch)

LUT4:I1->O 2 0.205 0.616 mux1/Mmux\_out251 (pc\_in\_31\_OBUF)

OBUF:I->O 2.571 pc\_in\_31\_OBUF (pc\_in<31>)

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Total 5.453ns (3.274ns logic, 2.179ns route)

(60.0% logic, 40.0% route)

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Cross Clock Domains Report:

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Clock to Setup on destination clock alu\_control/ALU\_op[1]\_PWR\_8\_o\_equal\_3\_o

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| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

-----------------+---------+---------+---------+---------+

clk | | | 5.660| |

control/ALUop\_1\_G| | | 2.433| |

-----------------+---------+---------+---------+---------+

Clock to Setup on destination clock alu\_control/op\_2\_G

-----------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

-----------------+---------+---------+---------+---------+

control/ALUop\_1\_G| | | 1.526| |

control/Branch\_G | | | 2.075| |

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Clock to Setup on destination clock clk

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| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------------------------------+---------+---------+---------+---------+

alu\_control/ALU\_op[1]\_PWR\_8\_o\_equal\_3\_o| | 5.120| | |

alu\_control/op\_2\_G | | 5.668| | |

clk | 10.531| | | |

control/Branch\_G | | 2.368| | |

control/MemtoReg\_G | | 3.142| | |

control/RegDst\_G | | 2.839| | |

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Clock to Setup on destination clock control/ALUop\_1\_G

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | | | 4.632| |

---------------+---------+---------+---------+---------+

Clock to Setup on destination clock control/Branch\_G

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | | | 4.758| |

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Clock to Setup on destination clock control/MemtoReg\_G

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

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clk | | | 2.671| |

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Clock to Setup on destination clock control/RegDst\_G

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | | | 4.758| |

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Total REAL time to Xst completion: 28.00 secs

Total CPU time to Xst completion: 27.99 secs

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Total memory usage is 4510536 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 46 ( 0 filtered)

Number of infos : 8 ( 0 filtered)